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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/574,653	05/18/2000	Youngmin Kim	TI-29012	8503

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EXAMINER
LEE, HSIEN MING

ART UNIT	PAPER NUMBER
2823	9

DATE MAILED: 11/01/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/574,653	KIM ET AL.
	Examiner	Art Unit
	Hsien-Ming Lee	2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 August 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) *13-19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Remarks

1. The 112-first-paragraph rejection to claims 4-12 is withdrawn in response to applicant's arguments filed 8/12/02.

2. Claims 1-19 are pending in the application. Of the above claims 13-19 are non-elected.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 1-6, 8-10 and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Dawson et al. (US 5,963,803).

With respect to claims 1-3, Dawson et al. in Figs. 1A-1L and related text expressly and inherently teach the claimed method of forming a CMOS sidewall spacer, comprising the steps of:

- forming a PMOS transistor gate structure 122 on a n-type region 108 of a semiconductor substrate 102 (Fig.1C);
- forming a NMOS transistor gate structure 120 on a p-type region 106 of the semiconductor substrate 102 (Fig.1C);
- forming single layer sidewall structure (an oxide layer; col. 6, lines 47-54) adjacent to the NMOS gate structure 126 and the PMOS transistor gate structure 122 (Fig.1H); and
- anisotropically etching the single layer sidewall structure adjacent to the NMOS transistor gate structure 126 such that the width of the single layer sidewall structure adjacent to the NMOS transistor gate structure (i.e. 144, which is 500 Å) is less than the width of the single layer sidewall structure adjacent to the PMOS transistor gate structure (i.e. 146, which is 800 Å) (col.6, lines 66-67) .

With respect to claims 4-6, 8-10 and 12, Dawson et al. also teach the claimed method of forming a CMOS sidewall spacer, comprising the steps of:

- providing a semiconductor substrate 102 of a first conductivity type such as p-type (col. 4, lines 63-64) with a region of a second conductivity type such as n-type region 108;
- forming a gate dielectric 112 on the semiconductor substrate 102;
- forming a conductive layer 114 on the gate dielectric 112 (Fig.1A);
- etching the conductive layer 114 and the gate dielectric 112 to form a first transistor gate stack (NMOS) with an upper surface on the semiconductor substrate 102 of a first conductivity (p-type) and a second transistor gate stack (PMOS) with an upper

surface on the region of semiconductor substrate of a second conductivity type (n-type, i.e. the N region 108) (Fig.1H);

- forming at least one single layer sidewall structure or film (an oxide layer) over the semiconductor substrate 102;
- anisotropically etching the single layer sidewall film such that all of the sidewall film is removed from the upper surface of the first transistor gate stack 126 (NMOS) and the upper surface of the second transistor gate stack 122 (PMOS), wherein a plurality of single layer sidewall structure of a first width 146 are formed adjacent to the second transistor gate stack 122 (PMOS), and a plurality of single layer sidewall structure of a second width 144 are formed adjacent to the first transistor gate stack 144 (NMOS) (Fig.1H);
- masking the second transistor gate stack 122 with a photoresist pattern 148 used for source drain implantation (Fig. 1I); and
- etching the single layer sidewalls of the first width adjacent to the first transistor gate stack 126 (NMOS) thereby forming single layer sidewalls of a second width adjacent to the first transistor gate stack 126 (NMOS), wherein the second width 144 is less than the first width 146 (Fig.1H).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 7 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dawson et al. (US'803) in view of Wang et al. (US 6,020,231).

Dawson et al. fail to teach utilizing a plasma etch process as the anisotropical etching for forming the sidewalls at both sides of the PMOS and the NMOS.

However, the plasma etch is a well-known practice for etching a sidewall film to form the sidewalls of the CMOS, as evidenced by Wang et al., in which they states that " a conventional fabrication technique for forming such side wall spacer is by way of CVD forming of an oxide layer, and a subsequent step of anisotropic etching, typically either reactive ion etching or plasma etching." (col. 1, lines 40-43).

Therefore, it would have been obvious to one of the ordinary skill in the art at the time of the invention was made to use the plasma etch process of Wang et al. to anisotropically etch the sidewall film of Dawson et al. to form the sidewalls of the PMOS and the NMOS since the plasma etch process is a reliable method for selectively etching with good dimension control.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-Ming Lee whose telephone number is 703-305-7341. The examiner can normally be reached on M-F (9:00 ~ 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are 703-305-0142 for regular communications and 703-305-0142 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Hsien Ming Lee
October 29, 2002

Olik Chaudhuri
Supervisory Patent Examiner
Technology Sector 2800